

Efficient Implementation of CELP-based speech coders on TMS320C64X processors

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Speech codecs play a vital part in modern wireless and wireline telephony (VoIP etc.) systems. Speech compression technology has progressed a long way from simple algorithms like the non-linear quantization (A-law, μ -law) to highly sophisticated vocoders such as G.723.1, G.729AB, GSM-AMR, HVXC etc, which achieve a compression ratio as high as 85 while still providing good speech quality. The price for these efficient speech compression algorithms is a significant increase in computational complexity. High performance DSPs are used to meet the computational needs in the infrastructure and handheld segments of the telephony systems. Speech codecs implementations for infrastructure applications (like the wireless base-stations and voice gateways) are critically evaluated by offered cost-per-channel in a multi-channel environment, which drives the need for highly optimized implementations.

Texas Instruments' TMS320C64xTM (C64xTM) is a processor targeted at broadband infrastructure and imaging applications. TMS320C64x processor belonging to C6000 DSP family and features TI's VelociTI.2TM VLIW architecture with support for wider data paths, larger register files, packed data processing (SIMD).

This paper presents an analysis of CELP based speech compression algorithms primarily ITU-T G.723.1 and techniques for achieving optimal performance in minimal time on Texas Instruments' TMS320C64xTM processor, by effective use of instruction set, functional units, pipeline, enhanced register file, advanced VLIW (VelociTI.2TM) architecture and development tool set.

Firstly an overview of generic Code Excited Linear Prediction (CELP) algorithm is given along with the description of major blocks of the encoder and decoder. This is followed by a brief overview of the ITU-T G.723.1 algorithm, which is a dual rate speech coder working on the principles of Algebraic CELP (ACELP) for the lower bit rate and Multi Pulse Maximum Likelihood Quantization (MP-MLQ) for the higher bit rate.

Next, the module wise complexity of G.723.1 speech codec is analyzed and quantified. This is supplemented with the processor loading and profile information on TI's C64x and Pentium processor. The profile results are used for processor load and code size information. With the help of these parameters a formula is derived for prioritization of the blocks to be optimized in minimal time.

Next, we present the techniques that are used for optimization of CELP modules on TI's C64x platform. These techniques are divided into two parts - quick optimizations and core optimizations. Quick optimizations rely on the compiler capabilities to yield very good results with minimal effort and time. These include usage of intrinsics, code optimization and restructuring to take benefit of the processor architecture. Even with these optimizations it is very difficult to generate optimal code for C64x, as the compiler needs to exploit the fine-grained parallelism in a sequential code. These sophisticated optimization techniques are described in detail under core optimizations, with sample implementation of filters, dot product and multiply-accumulate intensive loops.

The final section presents the results of different techniques used in the optimization of the ITU G723.1. As the code structure of CELP based algorithms are similar, the optimization techniques covered in this paper can be applied to other CELP codecs, resulting in efficient implementation on C64x with reduced development time.