

MPEG-2 to H.264 Transcoder on TI TMS320DM642

Arvind Raman, Kismat Singh, Manisha Agrawal Mohan,
Neelakanth Shigihalli, Sriram Sethuraman, B. S. Supreeth

Ittiam Systems (Pvt.) Ltd., Bangalore, India

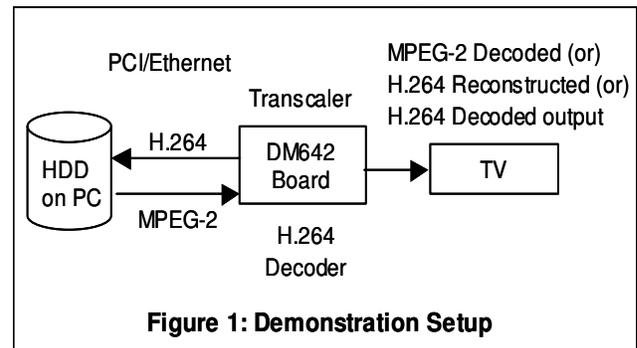
Email: sriram.sethuraman@ittiam.com

The technology behind H.264, a joint video coding standard by ITU-T and ISO, offers a significant reduction in bit-rate over earlier standards-based technologies such as MPEG-2 and MPEG-4. It offers a nearly 50% reduction in bitrate over MPEG-4 Advanced Simple Profile tools and a nearly 65% reduction in bitrate over MPEG-2 Main Profile tools at a comparable quality. Such a compression efficiency advantage spurs its adoption in personal video recorders (to increase the hours of stored content) and in network edge servers that stream content over various last mile solutions that have limited bandwidth. This requires transcoding from an MPEG-2 format which is the most prevalent format that is used in terrestrial/satellite/cable transmission of digital television content. The compression advantage, however, comes at the expense of three to four times higher computational complexity for the various coding tools employed in H.264.

The substantial difference between MPEG-2 and H.264 necessitates almost a complete decoding followed by a re-encoding solution, instead of a compressed domain or minimal draft based low-complexity transcoding solution. In this demonstration, we present an embodiment of a low-complexity MPEG-2 to H.264 transcoding algorithm. The algorithm leverages coding information from the MPEG-2 bitstream to reduce complexity of re-encoding in the H.264 format. H.264 coding tools such as spatial intra prediction, segmented motion compensation on macroblocks, CAVLC/CABAC, and quarter sample motion compensation have been leveraged to reduce the bit-rate of the MPEG-2 stream by 25% without any significant loss in visual quality. Further, by adapting the algorithms to work within a transcaling framework (e.g. MPEG-2 D-1 to half D-1 H.264), the compression advantage is stretched further.

In this demonstration, we will present a general-purpose DSP based solution implemented on TI's TMS320C642 processor. This DSP consists of a TI C64x VLIW core integrated with a 64-bit wide external memory interface, a 2-level memory hierarchy (16kB each of L1 Program and Data caches + 256kB of integrated L2 memory that can be configured as internal SRAM and L2 cache), an enhanced DMA controller with 64 programmable channels, and digital video and

audio input/output ports. The TI C64x is a VLIW (Very Long Instruction Word) architecture with 8 functional units (across two data paths) that can each execute an instruction on the same clock cycle. Each datapath has a .L (logical), .D (data), .M (multiplier), and .S (shift) unit and 32 32-bit registers. Access from one datapath to the other datapath is also supported. Some of these functional units further support SIMD instructions that are customized for packed byte or half-word operations that are very useful in handling video data. The D units are capable of loading or storing two 64-bit aligned data or one 64-bit unaligned data (which is again very useful during motion compensation) in one clock cycle. All instructions can be conditionally executed using 5 conditional registers. An ethernet MAC and PCI interface are also built on the device. The processor is capable of running at clock speeds of up to 720 MHz, and the C64x core has been tested at up to 1GHz.



The demo setup is illustrated in Figure 1. The demonstration will be shown using a TI DM642 based board that includes video/audio DACs and an ethernet port. The compressed MPEG-2 bitstream will reside on the hard disk of a PC and will be streamed to the transcoder via the PCI or the ethernet. The DM642 will decode the MPEG-2 and will transcode and trans-scale it to the H.264 format. This bitstream will again be streamed to the same hard disk over PCI or ethernet. The display can be chosen such that the decoded MPEG-2 stream or the H.264 reconstructed frames can be selected to be viewed on a television. Later, the transcoded bitstream will also be accessed from the hard disk, decoded, and displayed on the same DM642 board. The various resolution and bit-rate setting modes will be demonstrated.