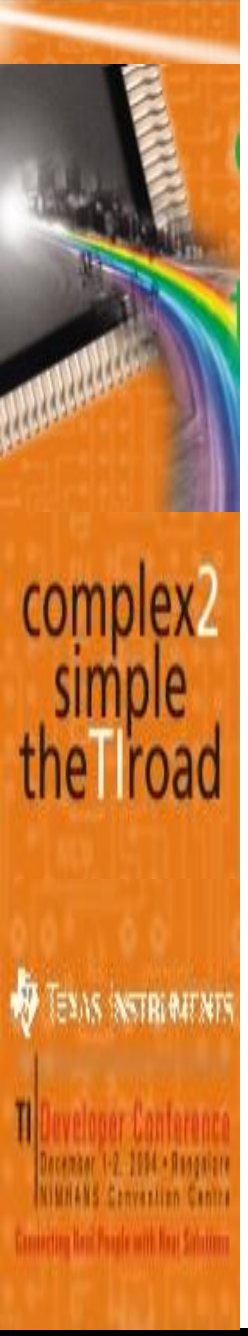
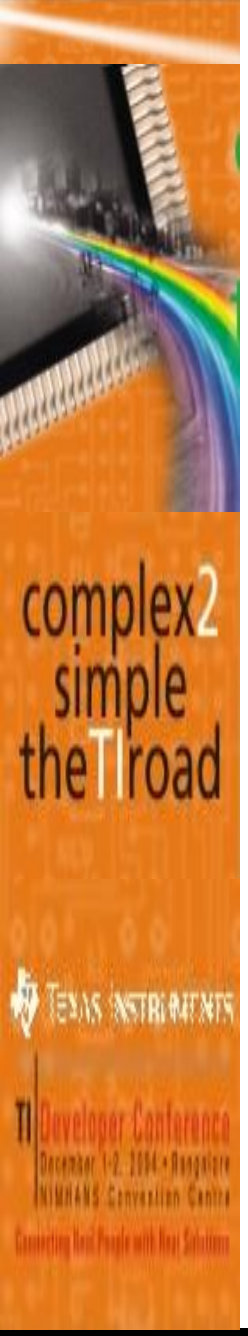


IP Video Phone on DM64x

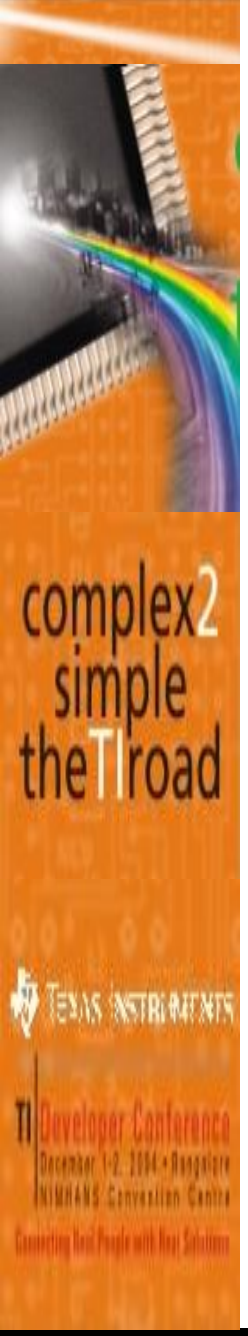
Sriram Sethuraman
Ittiam Systems Pvt. Ltd., Bangalore

Acknowledgments to:
Ittiam AV Systems and VVOIP Teams



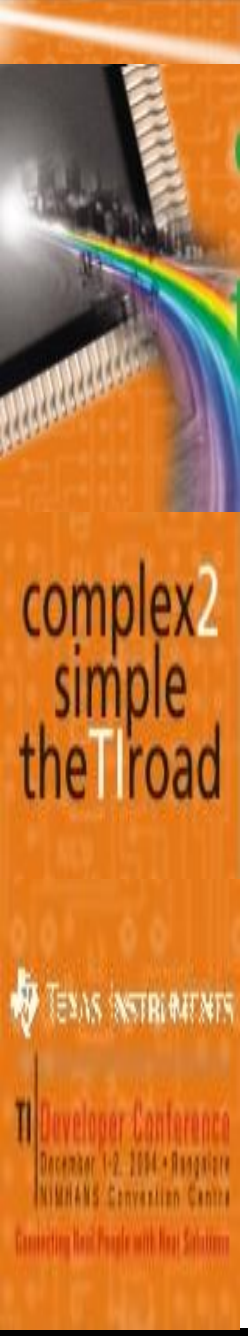
Overview

- Video Phone
  - Brief history
  - Over IP – New Markets
- Suitability of DM64x
  - Solution variants
- Challenges
  - Raw Computational Complexity
  - Interoperability
  - Quality of Service
    - Video Quality, Latency, Error Resilience, Lip Sync
  - Total Bill of Materials
- Ittiam Solution on DM642



Video Phone

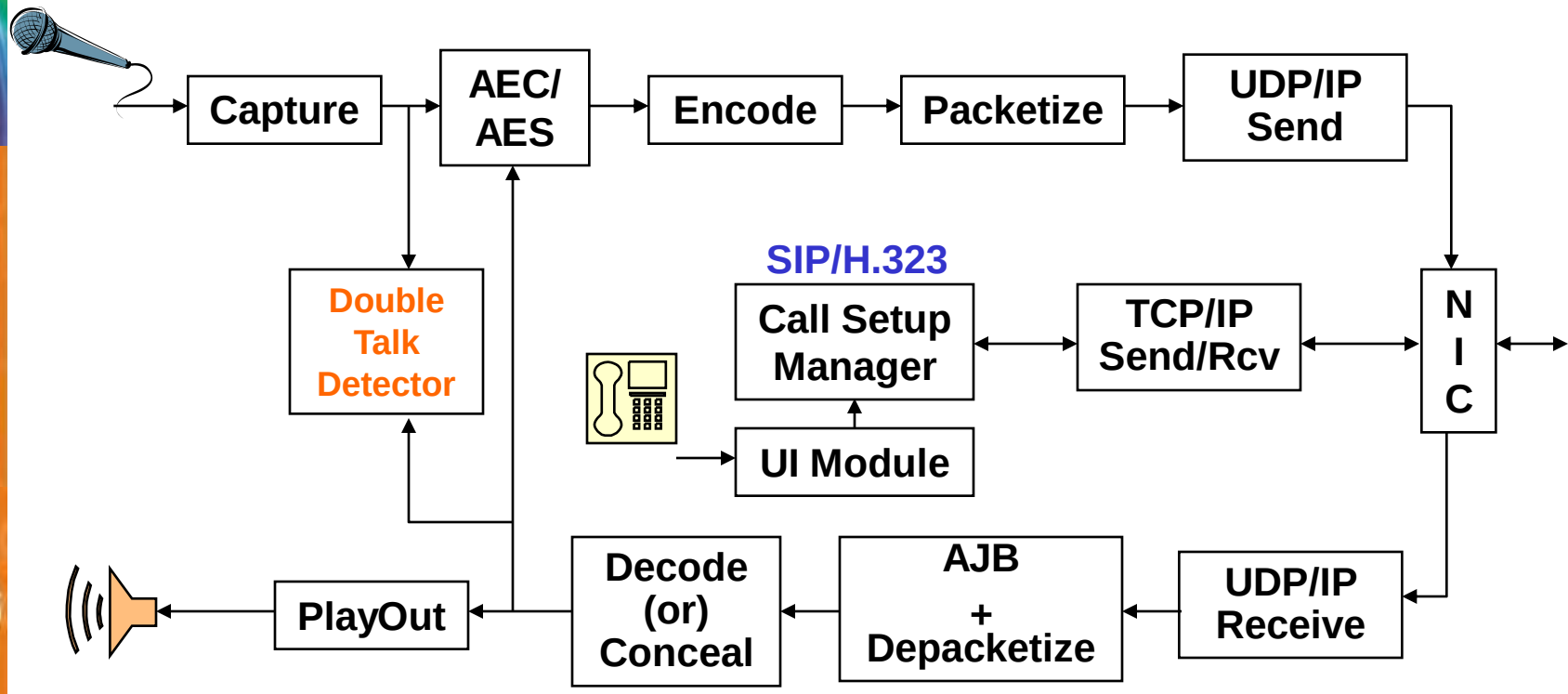
- Pursued since the 1960's
- Adopted widely today in corporate environments
  - Over ISDN
  - Over Leased networks
- Tends to be expensive
  - Cheap ones have poor quality
- PC software solutions exist for consumers
  - Hog most of the PC when running
  - High resolutions are not possible
    - Even if bandwidth permits it
  - Not TV-centric
- Bandwidth limitations to consumers
  - Limits the user experience



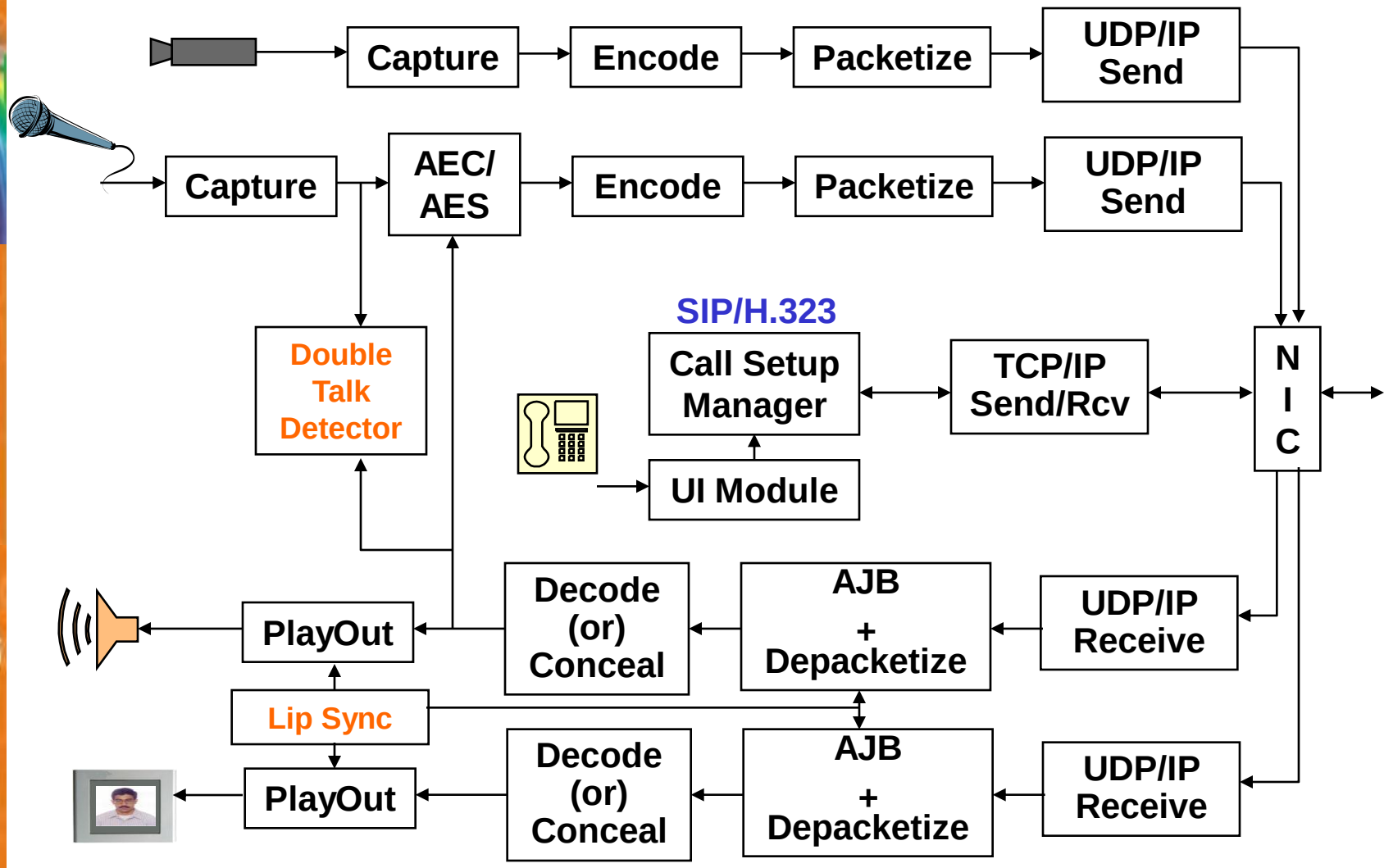
IP Video Phone

- Rides on the success of Voice over IP's wide acceptance
- Triggered by
  - Broadband deployments and last-mile solutions
    - DSL
    - DOCSIS cable modems
    - Wi-Fi/WiMax
  - Low cost computing power
  - High level of peripheral integration (reduced BoM)
  - Interoperability protocols
- New markets
  - Multi-use appliances (targeting the consumer space)
    - IP video phone / set-top box / …
  - PC acceleration cards (targeting the enterprise space)
    - For collaborative work environments
  - Video Acceleration for existing VoIP products

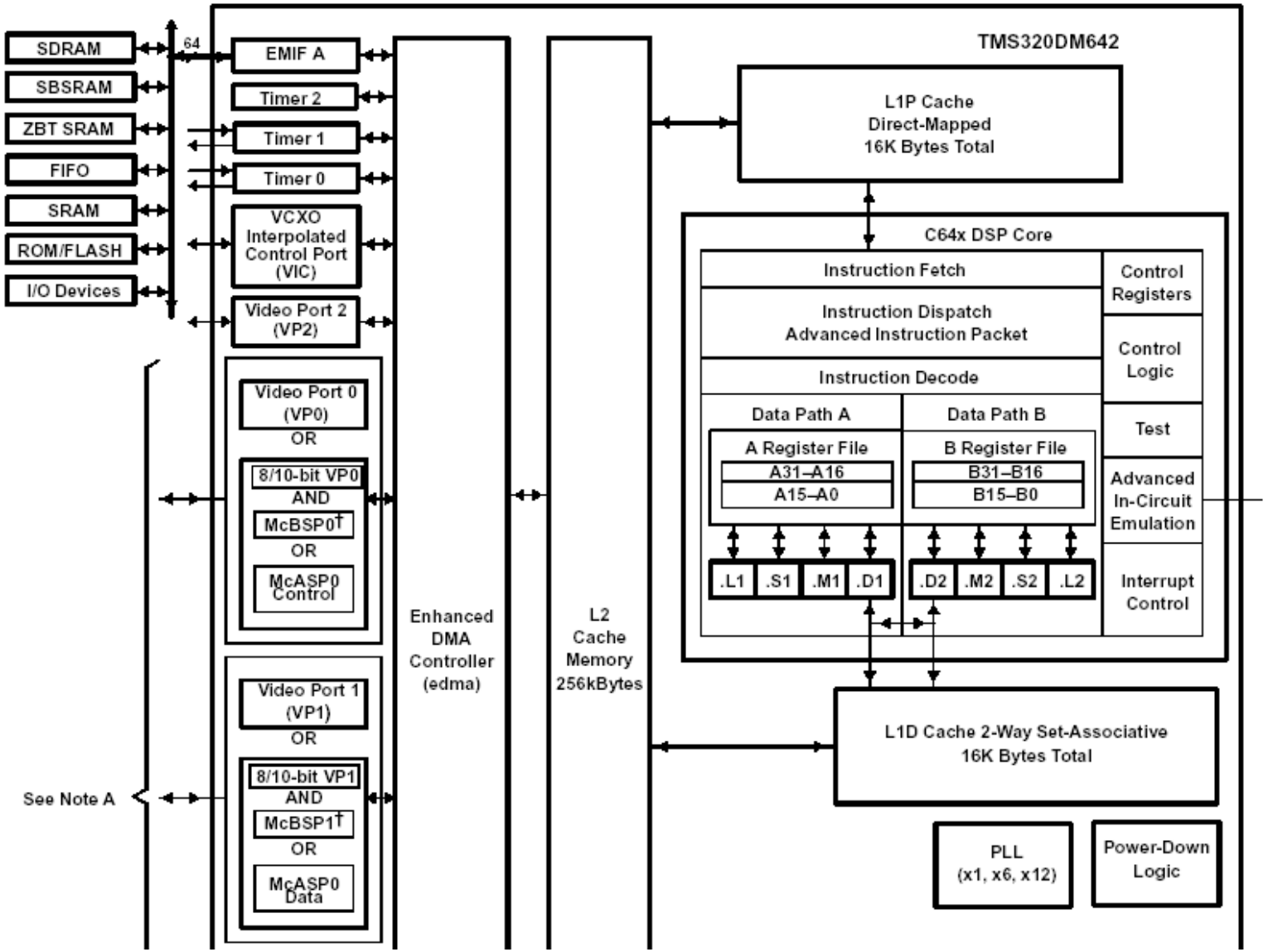
VoIP Components



VoIP + Video



TI TMS320DM642



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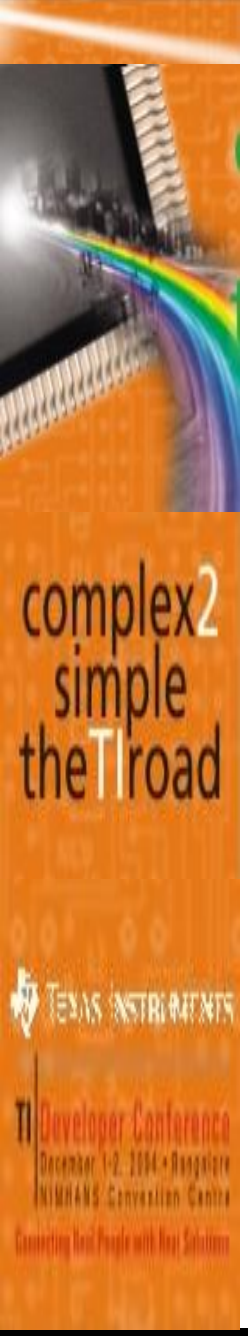
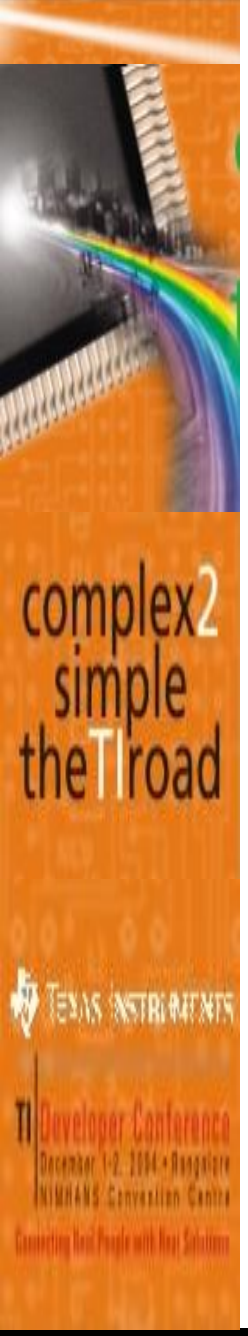


TI C64x DSP Core

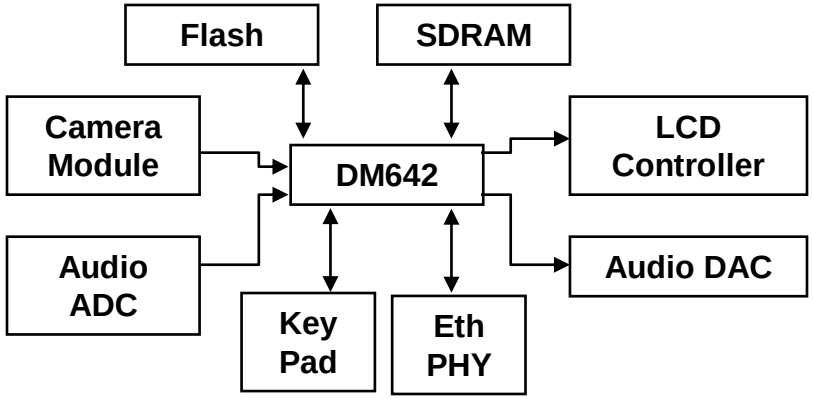
- Up to 1GHz clocking of the core
- VLIW architecture – exploits instruction level parallelism
- Acceleration for video compression
  - 8-bit SIMD instructions tuned for motion estimation/compensation
    - SUBABS4, AVGU4, MPY4 , etc.
  - Unaligned loads
  - Packing/unpacking instructions
  - 64-bit wide load/store
  - Enhanced DMA Controller
    - 2D DMA support
    - 4 Priority Queues (to allow peripherals to work in parallel)
    - 64-channels
    - Transfer Completion Interrupt, Chaining, & Linking
  - 2-level on-chip cache
    - Reasonable amount of on-chip memory



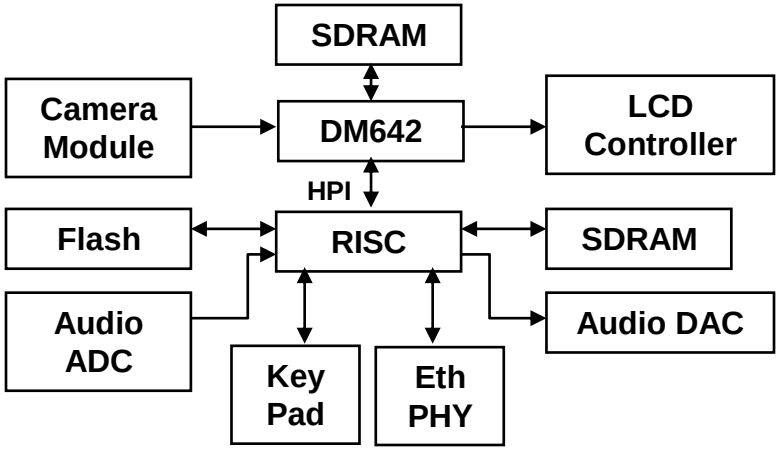
Suitability of TI DM641/642

- Glueless interface
  - to CMOS sensor modules
  - to LCD module or NTSC/PAL encoders
- I2C interface to control on-board peripherals
- On-chip Ethernet MAC with DMA capability
- PCI interface
  - Low cost peripherals
  - Easy to make it as an accelerator card
- Host Port Interface
  - Enables VoIP processor + Video processor model
- Interface to audio ADC and DAC
- Up to 64-bit wide EMIF
  - Enables code and data to be transferred faster
- GIOs for Keypad/Remote Interfacing

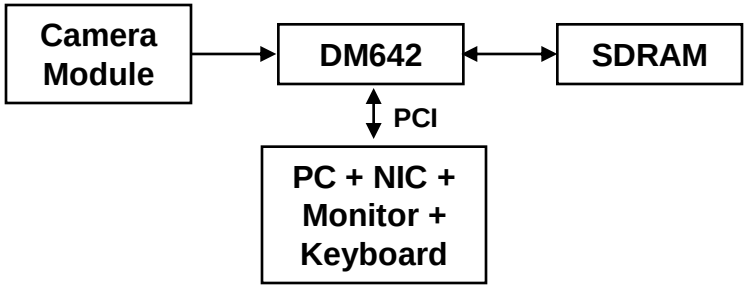
Potential Configurations



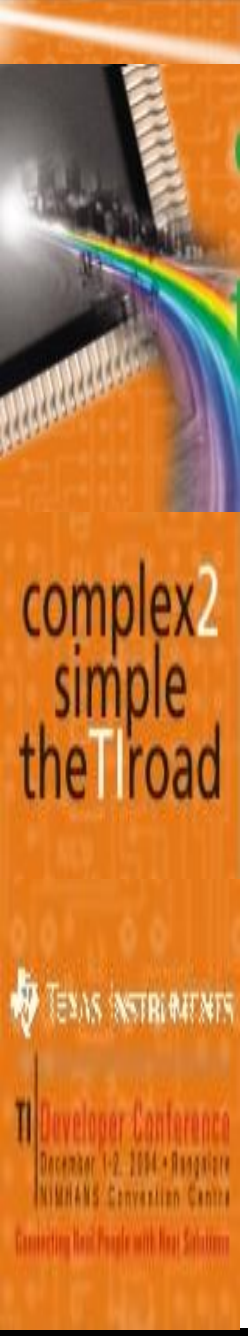
Single Processor



VoIP Processor + DM64x for Video Processing



PC (as VoIP Processor) + DM64x for Video Processing



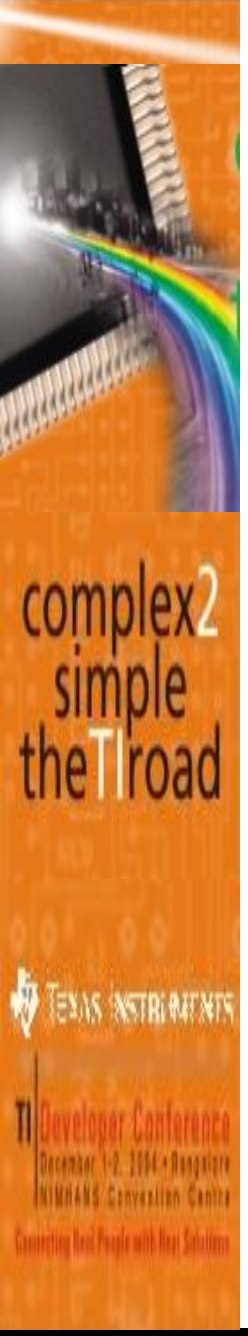
Challenge Dimensions

- To decrease network bandwidth requirements
  - Need to
    - Improve encoding algorithms
    - Move from H.263+/MPEG-4 to H.264
  - Increases computational complexity several fold

- So many pieces to integrate; Increases
  - Overall design complexity
  - Task scheduling complexity
  - Internal memory usage complexity
    - Code placement
    - Scratch re-use

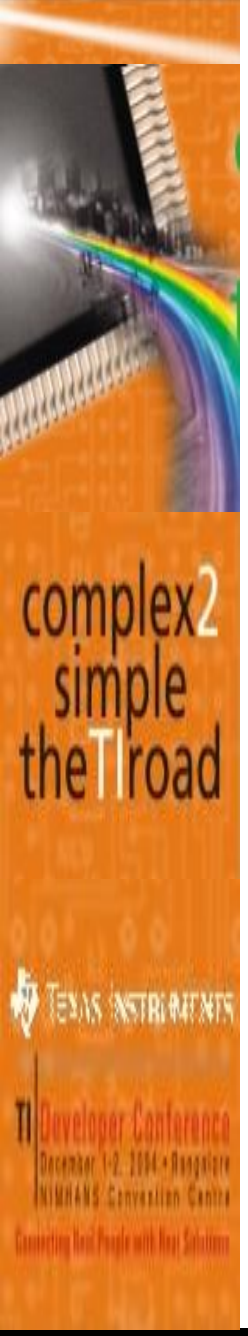
Challenge Dimensions

- Interoperability Challenges
  - Suite of Video and Speech Codecs
    - H.261, H.263, H.263+, H.264
    - G.711, G.723, G.726. …
  - RTP packetization for each codec
    - Variations introduced by different vendors
    - Draft stage for new codecs
  - SIP level interoperability
  - RTCP provision at the remote end
  - NTP server



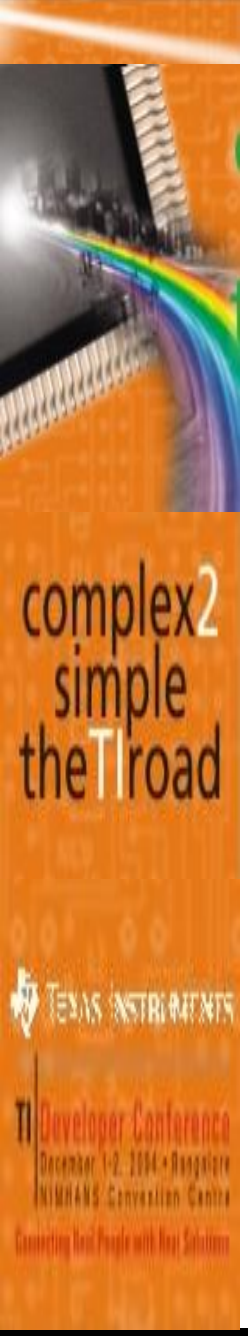
Challenge Dimensions

- Quality of Service Challenges
  - Visual quality
    - Complex encoding algorithms
    - In the presence of packet losses
      - Error robustness varies with the codec
      - Trade-offs among intra refresh rate, FEC protection, bit-rate, and quality
  - Latency
    - Needs to be close to 250ms for good interaction
    - Requires a fine granularity of scheduling to pipeline all processing stages
    - Have no control on Network latencies
    - Ability to respond to congestion through rate control



Ittiam Video Phone Solution

- DM642@600MHz based
- MPEG-4/H.263 at VGA@20-25fps + G.723
- All VoIP components
- Latency < 300ms (excluding network latency)
- Handles packet loss
  - ➔ through intra refresh, RTCP
- Custom reference board with camera, LCD, keypad, and speakers



Future Steps

- H.264 Baseline Profile@CIF@30fps
  - ➔ Exploit error resilience mechanisms in H.264
- Make it work with the multiple configurations
- Reduce latency through fine granular pipelining