Modeling, Analysis and Control of a Chain Cell Converter

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***Abstract*—Chain cell converter as a shunt connected, multilevel voltage source converter has been proposed for static VAR compensation. This converter consists of identical H-Bridge Building Blocks (HBBBs) connected in series in each phase. Chain cell converter synthesizes a desired ac waveform from several levels of DC voltages provided by the DC capacitors with only one switching per cycle. The transient model of the converter is developed considering a three phase three wire system. The analysis and design of converter controls is presented. DC voltage balancing strategy which involves pulse swapping is implemented. Simulations are carried out for the performance evaluation of converter controls. Chain cell converter is also tested, when connected in a distribution system, as a STATCOM to compensate the voltage flicker due to an arc furnace load.**

I. Introduction

SHUNT connected static compensators (STATCOM) are increasingly applied for fast reactive power compensation, control of voltage flicker and active filtering. In addition to pulse width modulated, two level (voltage source) converters, multilevel converters can also be considered for generating sinusoidal waveform for these applications. A chain cell converter constructed with H-Bridge Building Blocks (HBBBs) connected in series in each phase, forms a cascaded multilevel converter [1-4]. The chain cell converter synthesizes a desired ac waveform from several levels of DC voltages provided by DC capacitors with only two switching per cycle. The chain cell converter has the following advantages [5]. 1. It is energy efficient due to less switching losses compared to Pulse Width Modulated (PWM) converters. 2. It is cost effective as phase shifting transformers are not required as in multipulse converters. 3. Less device count as compared to multilevel diode clamp converters. 4. Less capacitor count as compared to multilevel flying capacitor converter. 5. With a suitable choice of firing angles the lower order harmonics can be completely eliminated. 6. Because chain links switch in sequence, the maximum voltage excursion of the converter waveform is limited by the number of switches in series. Therefore, radio interference is minimised. This paper deals with modeling, analysis and control of seven level chain cell converter, which can be extended to any number of levels.

The structure of single phase, seven level chain cell converter which consists of three cells connected in series is shown in Fig. 1a. Each cell comprises an H-bridge with its own capacitor charged to an initial voltage of V_{dc}, as shown in Fig. 1b. Each cell generates a three level output voltage comprising $+V_{dc}$, 0 and $-V_{dc}$. As all the cells in a phase are connected in series, the ac output voltage E_c, is the summation

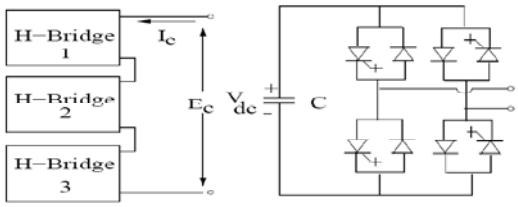

Fig. 1. (a) Seven level chain cell converter. (b) H-bridge that forms the cell.

of output voltages of each of the cells. A stack of n_c cells per phase produces $(2n_c+1)$ level symmetrical staircase voltage waveform, which gives a better approximation to a sine wave. The output voltage of the single phase, seven level converter is shown in the Fig. 2a. The phase current I_c will be either leading or lagging the phase voltage E_c by 90^0. The average charge to each capacitor is zero over half cycle. Because of

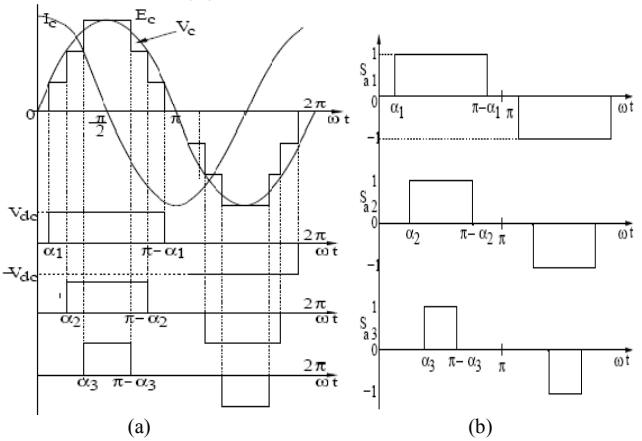

Fig. 2. (a) Seven level output voltage of a chain cell converter. (b) Switching functions for each cell.

this symmetric charge flow, the average voltage on all the capacitors remain constant at V_{dc} in steady state. The phase output voltage is controlled by controlling the firing angles of each of the cells. The fundamental component of output

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voltage, E_c, decides the compensating current I_c. Fig. 2b shows the switching functions of each cell in a single phase seven level converter. The Fourier expansion for the switching functions S_{a1}, S_{a2}, and S_{a3} are as follows

$$S_{a1}=\frac{4}{\pi}\sum_{n=1,3,5...}^{\infty}\frac{1}{n}[\cos(n\alpha_1)]\sin(n\omega t) \quad (1)$$

$$S_{a2}=\frac{4}{\pi}\sum_{n=1,3,5...}^{\infty}\frac{1}{n}[\cos(n\alpha_2)]\sin(n\omega t) \quad (2)$$

$$S_{a3}=\frac{4}{\pi}\sum_{n=1,3,5...}^{\infty}\frac{1}{n}[\cos(n\alpha_3)]\sin(n\omega t) \quad (3)$$

The terminal voltage of a single phase, seven level chain cell converter is

$$E_c = S_a V_{dc} \quad (4)$$

Where, $S_a = S_{a1}+ S_{a2}+ S_{a3}$ and V_{dc} is the voltage across the individual DC capacitors.

II. Transient Modeling of Chain Cell Converter

Consider a three phase, three wire system as shown in the Fig. 3, where V_{can}, V_{cbn} and V_{ccn} represent the source voltages per phase with respect to its neutral point n and E_{caN}, E_{cbN}, E_{ccN} represent the three phase output voltage of a seven level chain cell converter with respect to its neutral point N.

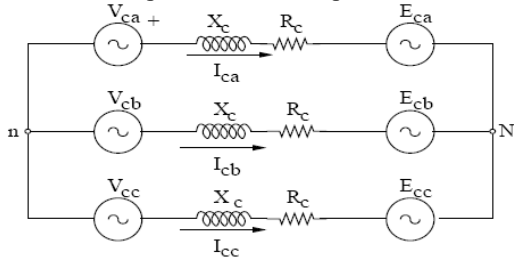

Fig. 3. A three phase three wire system.

Considering the phase 'a' of the system, we can write

$$V_{can} = L_c\frac{dI_{ca}}{dt} + R_c I_{ca} + E_{can} \quad (5)$$

where, E_{can} is the converter output voltage with respect to the source neutral n. E_{can} can be written as

$$E_{can} = E_{caN} + E_{Nn} \quad (6)$$

where, E_{Nn} represents voltage between the source neutral and the converter neutral. Similarly, for the other two phases,

$$E_{cbn} = E_{cbN} + E_{Nn} \quad (7)$$

$$E_{ccn} = E_{ccN} + E_{Nn} \quad (8)$$

Adding (6) - (8) and on rearranging, we arrive at

$$E_{Nn} = -\frac{E_{caN} + E_{cbN} + E_{ccN}}{3} \quad (9)$$

In deriving (9), it is assumed that the sum of the source voltage is zero (i.e. zero sequence component does not exist). The phase voltage of the converter with respect to its neutral N, for a seven level chain cell converter, according to (4) is,

$$E_{cjN} = S_{j1}V_{dc1}^{j} + S_{j2}V_{dc2}^{j} + S_{j3}V_{dc3}^{j} \quad (10)$$

where, j = a, b or c. The transient model of the three phase seven level chain cell converter for a three phase three wire system is obtained as

$$\begin{bmatrix} \frac{d}{dt}V_{dc1}^{j} \\ \frac{d}{dt}V_{dc2}^{j} \\ \frac{d}{dt}V_{dc3}^{j} \\ \frac{d}{dt}I_{cj} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{S_{j1}}{C_{j1}} \\ 0 & 0 & 0 & \frac{S_{j2}}{C_{j2}} \\ 0 & 0 & 0 & \frac{S_{j3}}{C_{j3}} \\ -\frac{S_{j1}}{L_c} & -\frac{S_{j2}}{L_c} & -\frac{S_{j3}}{L_c} & -\frac{R_c}{L_c} \end{bmatrix} \begin{bmatrix} V_{dc1}^{j} \\ V_{dc2}^{j} \\ V_{dc3}^{j} \\ I_{cj} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ \frac{1}{L_c} \end{bmatrix} V_{cjn} - \begin{bmatrix} 0 \\ 0 \\ 0 \\ \frac{1}{L_c} \end{bmatrix} E_{Nn} \quad (11)$$

where, the variables V^{j}_{dc1}, V^{j}_{dc2} and V^{j}_{dc3} in (10) and (11), represent the voltage across the capacitors C_{j1}, C_{j2}, C_{j3} respectively. S_{j1}, S_{j2}, S_{j3} represent the switching functions for j^{th} phase of the converter.

The three phase, three wire system described above is simulated for capacitive and inductive operation of chain cell converter. The system parameters used are listed in Appendix A. Fig. 4 shows current and voltage waveforms when the capacitive current is drawn by chain cell converter and Fig. 5 shows the waveforms when inductive current is drawn. Fig. 6 shows the converter neutral voltage with respect to the source neutral voltage i.e. E_{Nn}.

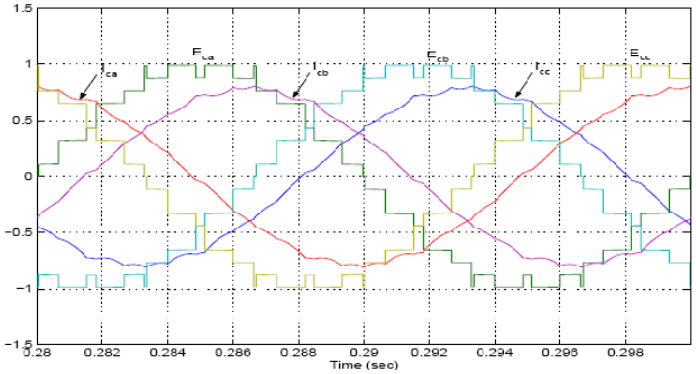

Fig. 4. Figure showing terminal voltages E_{ca}, E_{cb}, E_{cc} and the capacitive currents I_{ca}, I_{cb} and I_{cc} drawn by three phase seven level chain cell converter.

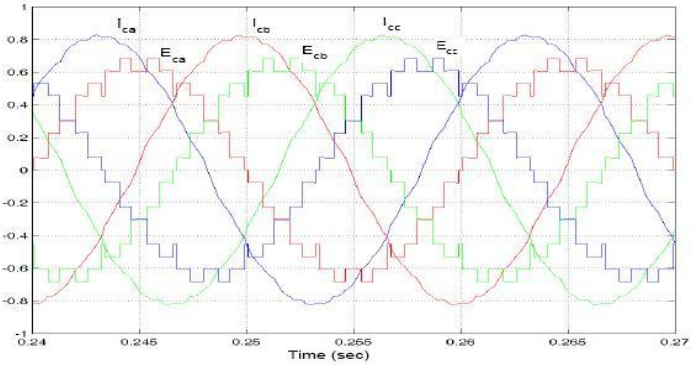

Fig. 5. Figure showing terminal voltage E_{ca}, E_{cb}, E_{cc}, and the inductive currents I_{ca}, I_{cb} and I_{cc} drawn by three phase seven level chain cell converter.

III. Analysis and Design of Controllers

The fundamental component of the converter terminal voltage has to be controlled so as to inject the desired reactive current. The terminal voltage is controlled by controlling the firing angles of the converter. The firing angles are derived from the current controller and DC voltage controller. The design of

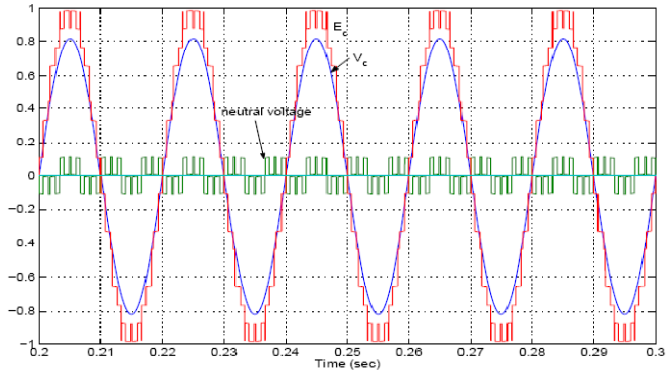

Fig. 6. Figure showing converter neutral voltage E_{Nn} along with terminal voltage E_{ca} and source voltage V_{ca} for phase 'a' of the converter.

decoupled current controller and DC voltage controller is done by considering the model of chain cell converter in d-q reference frame, which is based on the following assumptions. 1. The source voltage V_c is considered to be balanced and sinusoidal. 2. The switches are assumed to be lossless 3. The harmonics in the converter output voltage, E_c, are neglected. 4. All the capacitors are assumed to be lossless and the voltage across each of the capacitors is assumed to be constant at V_{dc}.

Consider a system where the chain cell converter connected to a bus through a reactor having an inductance L_c and resistance R_c as shown in Fig. 7a. There is no loss of generality assuming phase of source voltage as 0^0.

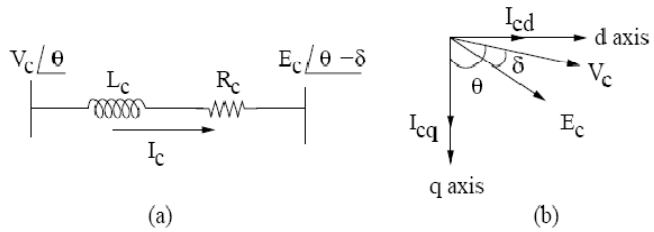

Fig. 7. (a) Equivalent circuit of compensator connected to the system. (b) Representation in d-q frame.

The equations for the circuit shown in Fig.7(a) (using d-q components) are given by,

$$L_c \frac{di_{cd}}{dt} + R_c i_{cd} = u_{cd} \tag{12}$$

$$L_c \frac{di_{cq}}{dt} + R_c i_{cq} = u_{cq} \tag{13}$$

where,

$$u_{cd} = v_{cd} - e_{cd} - \omega L_c i_{cq} \tag{14}$$

$$u_{cq} = v_{cq} - e_{cq} + \omega L_c i_{cd} \tag{15}$$

The equation for V_{dc} is given by

$$\frac{dV_{dc}}{dt} = \frac{k}{C}\left(i_{cd}\sin(\theta-\delta) + i_{cq}\cos(\theta-\delta)\right) \tag{16}$$

where,

$k = \sqrt{\frac{3}{2}}\frac{4}{\pi}\left[\cos(\alpha_1)+\cos(\alpha_2)+\cos(\alpha_3)\right]$ and $\frac{1}{C} = \frac{1}{27}\left(\frac{1}{C_1}+\frac{1}{C_2}+\frac{1}{C_3}\right)$.

C_1, C_2 and C_3 are the capacitances in three cells of each phase, respectively. The derivation of the relation in (16) is presented in Appendix B for reference. (12) (13) and (16) represent the model of chain cell converter in d-q reference frame. Control is achieved through variation of k and δ. The zero crossing bus voltage is taken as reference for the compensator voltages. The converter draws small real power to maintain the DC capacitor voltage. The instantaneous active and reactive power drawn will be $p_c = V_c\, i_{cd}$ and $q_c = V_c\, i_{cq}$. Therefore, i_{cd} and i_{cq} determines the active and reactive power components of the converter. This requires decoupled control of the two current components, i_{cd} and i_{cq}, in order to control real and reactive power components, p_c and q_c independently. To ensure this, the desired converter output voltages are given by

$$e^*_{cd} = v_{cd} - \omega L_c i^*_{cq} - u_{cd} \tag{17}$$

$$e^*_{cq} = v_{cq} + \omega L_c i^*_{cq} - u_{cq} \tag{18}$$

Fig. 8 shows the DC voltage and decoupled current controllers. The inner loops are the current control loops which generate the desired terminal voltage reference e_{cd}^* and e_{cq}^*. The outer loop is the DC voltage control loop which generates the current reference i_{cd}^* in order to control the DC voltage across each of the capacitors. The reactive current reference i_{cq}^* is determined according to the reactive compensation requirements.

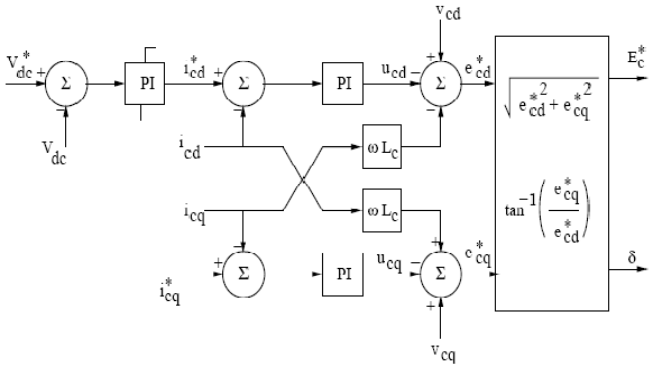

Fig. 8. DC voltage and decoupling current controllers.

The current controllers are of PI type and are designed using pole zero cancellation method. In designing the current controllers, converter delay is neglected. According to (17) and (18), the control variables u_{cd} and u_{cq} are obtained as outputs from two independent PI current controllers as shown in Fig. 9.

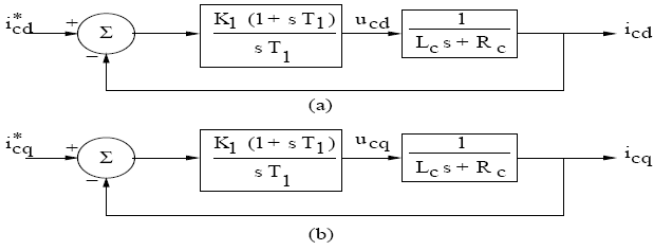

Fig. 9. (a) d-axis current controller. (b) q-axis current controller.

T_1 is chosen as $\frac{L_c}{R_c}$ to cancel the pole. $K_1 = \frac{L_c}{\tau_i}$, where τ_i is the desired time constant. The closed loop transfer function for the d-axis current i_{cd} and the q-axis current i_{cq} are

$$i_{cd}(s) = \frac{1}{\tau_i s + 1} i^*_{cd}(s) \tag{19}$$

$$i_{cq}(s) = \frac{1}{\tau_i s + 1} i^*_{cq}(s) \tag{20}$$

τ_i is chosen as 5ms. For this value of τ_i, the controller parameters will be K_1 = 0.127 and T_1 = 63.66msec. The purpose of DC voltage controller is to maintain a constant DC voltage across the capacitors by controlling the d-axis current reference of i_{cd}^*. The DC voltage controller is designed based on the small signal model about the operating point. In the analysis, the converter switches and DC capacitors are assumed to be lossless. We can write the power balance equation as

$$V_{dc} I_{dc} = e_{cd} i_{cd} + e_{cq} i_{cq} \tag{21}$$

About the operating point (i_{cdo},i_{cqo}), $e_{cdo} = kV_{dco}$, $e_{cqo} = 0$, $i_{cdo} = 0$ and $I_{dco} = 0$. Linearising (21) about the operating point, we arrive at,

$$\Delta I_{dc} = \frac{e_{cdo}\Delta i_{cd} + i_{cqo}\Delta e_{cq}}{V_{dco}} \tag{22}$$

The source voltage is assumed to be constant and the desired reactive current reference is also constant. So, $\Delta v_{cq} = 0$ and $\Delta i_{cq} = 0$. The small signal model for the converter about the operating point is obtained from (13) as

$$\Delta e_{cq} = \omega_o L_c \Delta i_{cd} \tag{23}$$

Substituting (23) in (22), we arrive at

$$\Delta I_{dc} = b_d \Delta i_{cd} \tag{24}$$

where, $b_d = k + \frac{\omega_o L_c i_{cqo}}{V_{dco}}$. The variation of b_d with the operating point, i_{cqo}, is plotted in Fig .10. The curve is plotted for k = 3.725, corresponding to minimum THD.

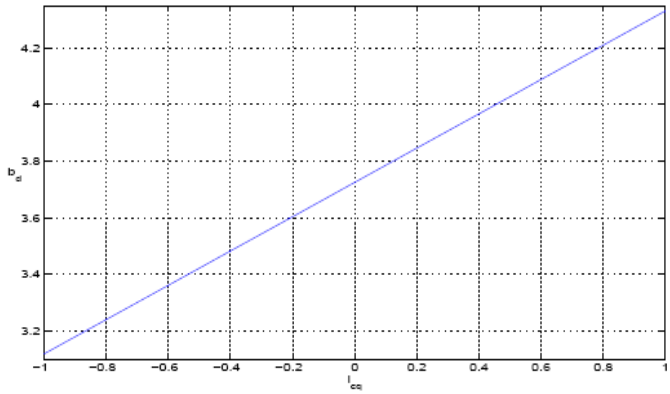

Fig. 10. Variation of b_d with reactive current i_{cq}.

The DC voltage controller K_p is designed based on the small signal model developed about the operating point. The analytical model of control loop for DC voltage is shown in the Fig. 11.

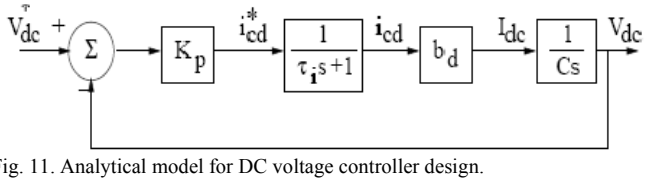

Fig. 11. Analytical model for DC voltage controller design.

The closed loop transfer function obtained for the DC voltage controller is

$$\frac{V_{dc}}{V_{dc}^*} = \frac{1}{\tau_i C} \frac{K_p b_d}{s^2 + \frac{1}{\tau_i} s + \frac{K_p b_d}{\tau_i C}} \tag{25}$$

The characteristic equation of the system is $s^2 + \frac{1}{\tau_i} s + \frac{K_p b_d}{\tau_i C} = 0$. τ_i determines the DC voltage controller settling time (T_s), according to the relation, $T_s = 9.2\tau_i$. From the characteristic equation, the damping ratio is $\zeta = \sqrt{\frac{C}{4K_p b_d \tau_i}}$. The DC voltage controller gain K_p is chosen as 40. The damping ratio ζ for the designed DC voltage controller will be 0.752, for the operating point of i_{cqo} = -1pu i.e. 1pu capacitive current drawn by the chain cell converter.

IV. DC VOLTAGE BALANCING STRATEGY

The wave forms of bus voltage V_c, converter terminal voltage E_c, and the current injected by converter, I_c, for phase 'a' of the converter are shown in Fig. 12. The phase current I_c will be either leading or lagging the phase voltage E_c by 90^0, when used as a STATCOM under normal conditions. The average charge to each capacitor will be zero over half cycle and thus the average capacitor voltage remains constant over a fundamental cycle. However, the DC voltage cannot be maintained due to switching and capacitor losses. If E_c is controlled such that it lags V_c by small angle δ, then the total real power flow into the converter is $\frac{V_c E_c}{X_c} \sin\delta$, where, X_c is the impedance of interface inductor. The phase shift of δ, is controlled by the outer DC voltage control loop as shown in Fig. 8. Since the conduction periods of each of the capacitors

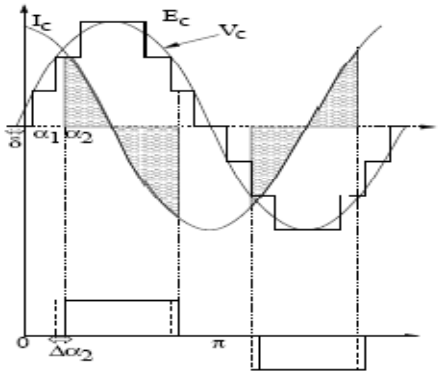

Fig. 12. Control of individual DC capacitor voltages.

in a phase are different, the switching losses are different and hence each DC capacitor voltage may not be exactly balanced with the outer loop only. Separate inner DC voltage control loops for each capacitor are necessary in order to maintain each of the capacitor voltages at V_{dc}. The purpose of inner control loop is to offset the real power flow to into each of the individual H-Bridges [2], which is achieved by shifting the switching patterns as shown in Fig. 12. The amount of charge flow due to phase shift of $\Delta\alpha_i$ is

$$\Delta Q_i = \int_{\alpha_i + \Delta\alpha_i}^{\pi - \alpha_i + \Delta\alpha_i} \sqrt{2} I \cos\alpha_i = 2\sqrt{2} I \cos\alpha_i \sin\Delta\alpha_i \tag{26}$$

where, i = 1, 2, 3...n_c. n_c is the number of capacitors per phase and I is the rms value of the line current. The charge flow into the i^{th} cell is proportional to $\Delta\alpha_i$. Thus, using an inner control loop, we shift the firing angle by $\Delta\alpha_i$ such that the capacitor voltages are balanced. The phase shifts are of the order,

$\Delta\alpha_i << \delta < 0.01$rad. The number of inner control loops required are equal to (n_c*3) for a three phase chain cell converter.

The disadvantages of using the above scheme for maintaining each of the capacitor voltages of a chain cell converter are 1. Unequal utilization of the switches. 2. Using capacitors of different values makes the selection difficult. 3. Large number of inner DC voltage balancing loops. There is also a problem of overcharging and under charging of capacitors, when the chain cell converter is used for harmonic filtering, as shown in the Fig. 13. In order to overcome these disadvantages, a new control strategy is proposed [6] for maintaining the capacitor voltages, where each capacitor of the converter produces voltage pulses of all widths as shown in the Fig. 14. The advantages of this pulse swapping technique are 1. We can use single value of capacitance in all the cells of the converter. 2. All switches are equally utilized. 3. The voltage across each of capacitors will be constant, thus eliminating the inner DC voltage balancing loops.

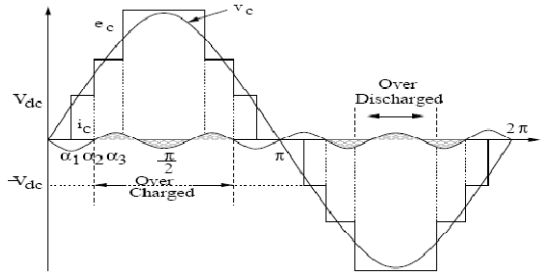

Fig. 13. Overcharging and overdischarging of capacitors.

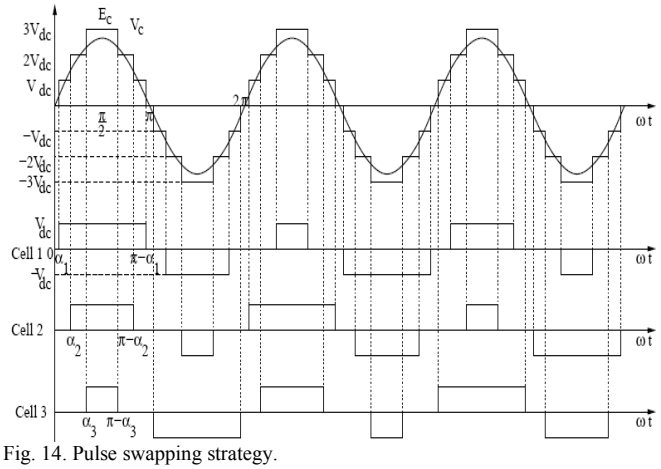

Fig. 14. Pulse swapping strategy.

V. PERFORMANCE EVALUATION OF CONVERTER CONTROLS

A. STATCOM connected to a voltage source

Fig. 8 shows the decoupled current control and DC voltage control strategy which generates the terminal voltage reference, E_c^* and the phase shift δ. Fig. 15 shows the block diagram for generating the firing pulses to each of the cells. The reference terminal voltage, E_c, generates the switching angles for each of the cells of chain cell converter through a switching pattern table. This table contains an array of possible terminal voltages of the chain cell converter and the corresponding firing angles for each of the cells. The pulse swapping logic will rotate the firing pulses every half cycle among the cells. The phase angle of source voltage, θ, is taken as reference for firing the switches. The converter controls are tested with step changes in current and DC voltage references and the simulation results are presented.

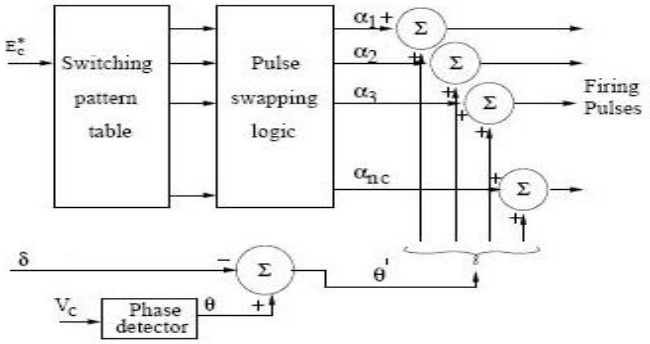

Fig. 15. Block diagram showing the generation of firing pulses.

The current controller is tested with step change in the current reference from capacitive current of 1pu to inductive current of 1pu at 0.35 sec and back to capacitive current of 1pu at 0.65 sec. The response of the current controller is shown in the Fig. 16. The waveform showing the transition from capacitive current of 1pu to inductive current of 1pu at 0.35 sec for phase 'a' of the converter is shown in the Fig. 17 and the transition from inductive current of 1pu to capacitive current of 1pu at 0.65 sec is shown in the Fig. 18. It is observed that the response of the current controller is quite rapid as expected and the settling time is a fraction of a cycle.

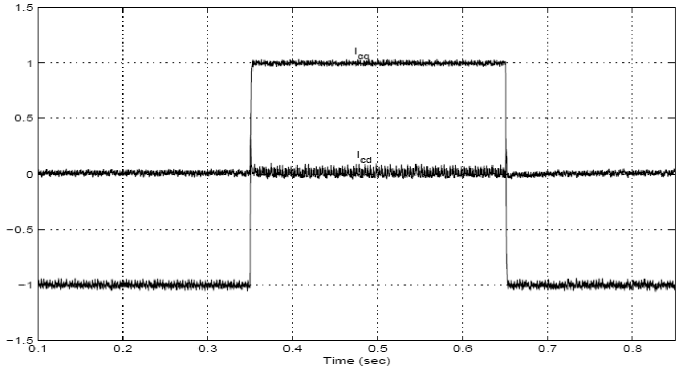

Fig. 16. Response for step change in the reactive current from capacitive to inductive and back to capacitive.

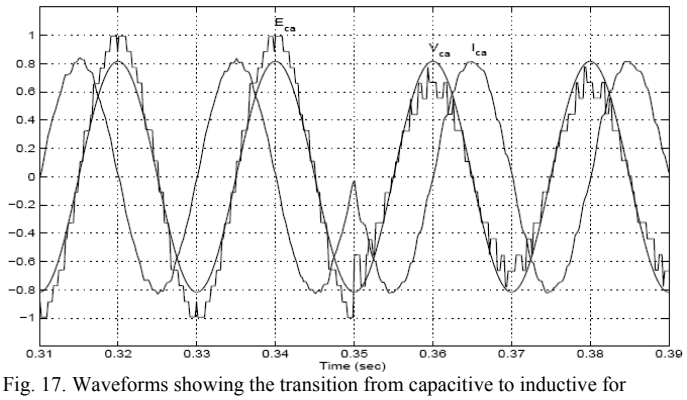

Fig. 17. Waveforms showing the transition from capacitive to inductive for phase 'a' of the converter.

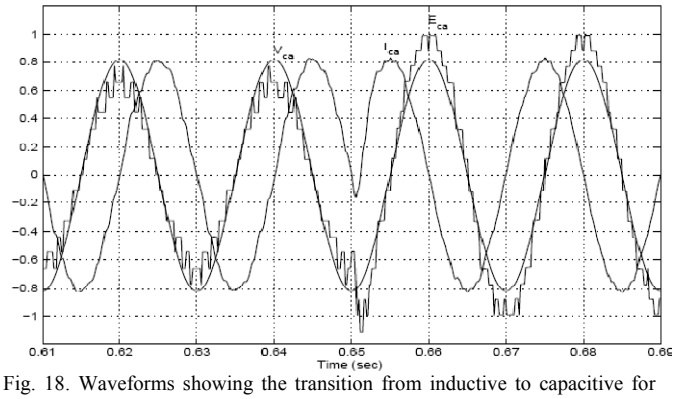

Fig. 18. Waveforms showing the transition from inductive to capacitive for phase 'a' of the converter.

Fig. 19 shows the response of DC voltage controller for a step change in DC voltage from 0.33pu to 0.35pu and back to 0.33pu. The DC voltage controller settling time is found to be 50msec as compared to 46msec computed theoretically.

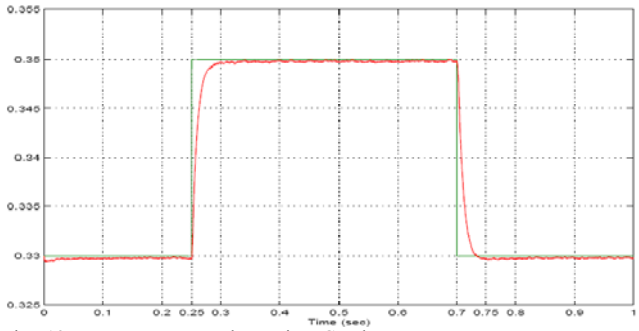

Fig. 19. Response to step change in DC voltage.

B. STATCOM as a compensator in a distribution system

An electric power system, shown in Fig. 20, is considered for reactive power compensation at PCC (Point of Common Coupling). It consists of an arc furnace supplied via HV/MV

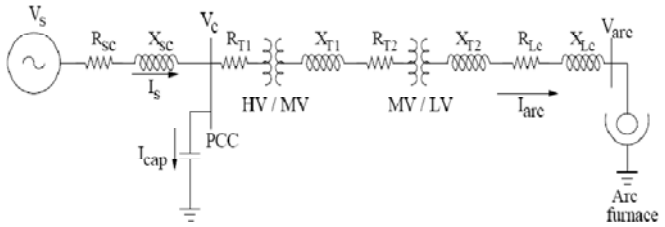

Fig. 20. Schematic of electric power system with compensator.

transformer from a transmission network. The MV/LV transformer supplies power to the arc furnace. Appendix A gives the system data. The arc furnace is a highly variable nonlinear load and produces voltage flicker in the distribution system. STATCOM connected at the PCC should inject the required compensating current such that source current becomes balanced and sinusoidal, thus, reducing the flicker at PCC. The compensation scheme, shown in Fig. 21, is used to generate the reference currents, i_{cd}^* and i_{cq}^*, for STATCOM, which will contain the harmonics, negative sequence and zero

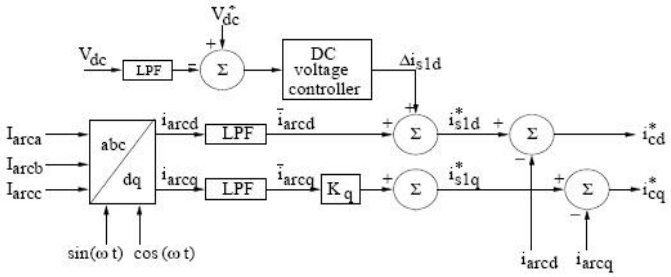

Fig. 21. Compensation scheme for generating the compensating current references.

sequence components of load current. The fundamental component of load current, which has to be supplied by source, is extracted using low pass filters. i_{s1d}^* and i_{s1q}^* represents the reference d-q components of the source current. The reference source currents are

$$i_{s1d}^* = \bar{i}_{arcd} + \Delta i_{s1d} \tag{27}$$

$$i_{s1q}^* = K_q \bar{i}_{arcq} \tag{28}$$

where, $K_q < 1$, is the degree of compensation used. The shunt capacitance connected at PCC is designed to supply half of the maximum compensating current required by the load. This is incorporated in the control strategy by taking K_q as 0.5. Δi_{sd1} represents the output of DC voltage controller. The reference currents for the converter, i_{cd}^* and i_{cd}^* are extracted by subtracting the load current from the source current.

$$i_{cd}^* = i_{s1d}^* - i_{arcd} \tag{29}$$

$$i_{cq}^* = i_{s1q}^* - i_{arcq} \tag{30}$$

Fig. 22 and Fig. 23 shows the simulation results for reactive VAR compensation at PCC. From Fig. 22, we can observe that variation in the magnitude of PCC voltage is 0.154pu before compensation. The chain cell converter is switched on at 0.6 sec to meet the compensation requirements. After compensation, the variation in PCC voltage is 0.066pu. From Fig. 26, we can observe that the magnitude of variation in source current reduces from 0.226pu before compensation to 0.1pu after compensation. The average magnitude of the source current is also reduced due to reactive compensation.

VI. CONCLUSION

In this paper, chain cell converter is proposed as a shunt connected STATCOM. The transient model of the chain cell converter is presented considering a three phase three wire system. The controllers for the chain cell converter are designed to inject the desired reactive current and regulate the DC voltage across the capacitors based on the small signal model developed about the operating point. Pulse swapping strategy is used to maintain the DC voltage across each of the capacitors constant. The control design is tested by transient digital simulation of the converter connected to a voltage source. The performance of the shunt connected chain cell converter in a distribution system, for the compensation of voltage flicker caused by an arc furnace, is also evaluated. The results validate the efficiency of the control design.

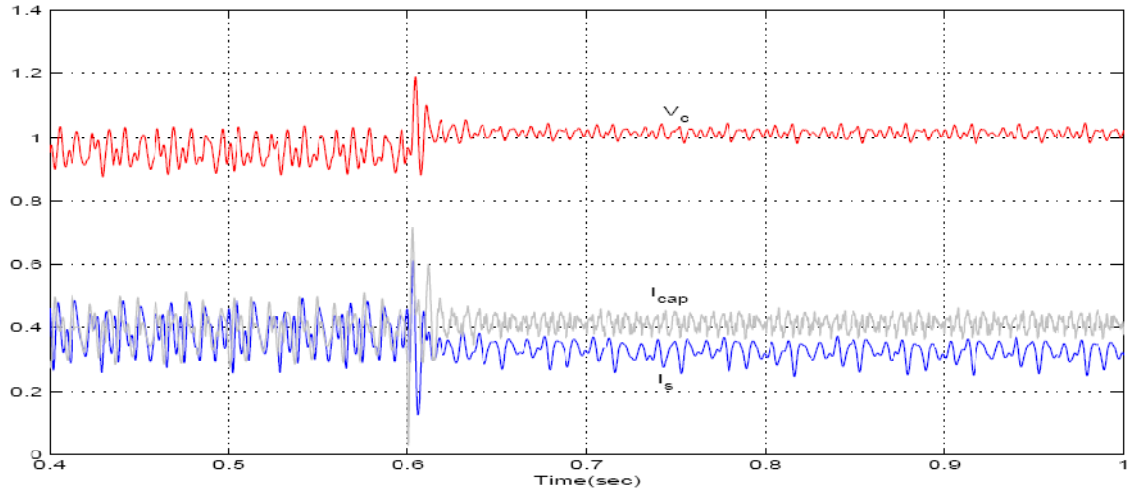

Fig. 22. Magnitude of PCC voltage V_c source current I_s, capacitor current I_{cap}.

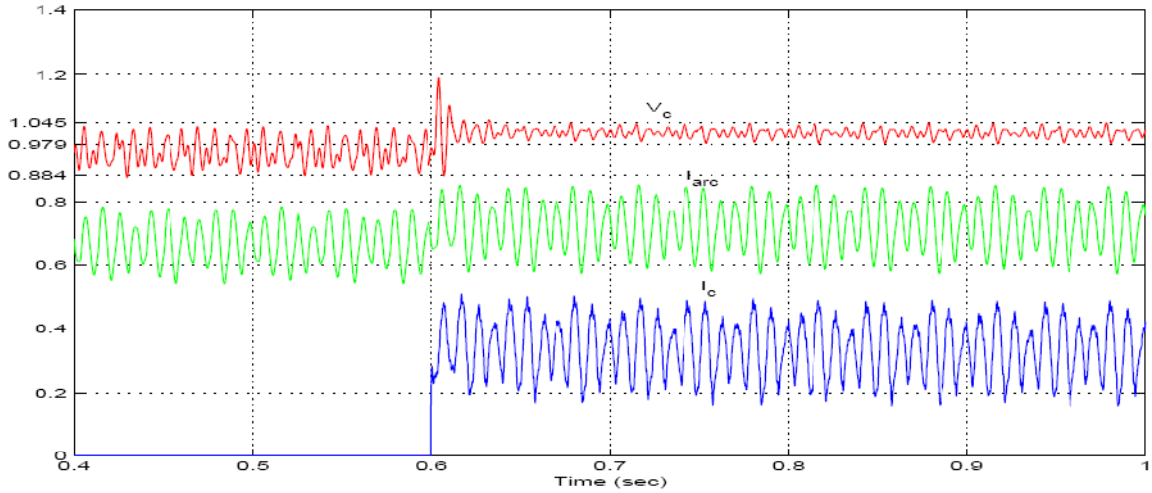

Fig. 23. Magnitude of arc current I_{arc} and compensator current I_c .

VII. Appendix A

Chain cell converter data:
F = 50Hz; ω = 2πf;
$X_c = \omega L_c = 0.2$pu; R_c=0.01pu;
capacitance in each cell: $b_c = \omega C_1 = 49.298$pu.
Note that $C_1 = C_2 = C_3$ using pulse swapping strategy.
Electric power system data:
V_s = 1pu; X_{sc}=0.2pu; R_{sc}=0.01pu; X_{T1}=0.1315pu;
R_{T1}=0.0066pu; X_{T2}=0.166pu; R_{T2}=0.0083pu; X_{Lc}=0.833pu;
R_{Lc}=0.083pu; b_{cap}=4.082pu.

VIII. Appendix B

Considering a chain cell converter with n_c cells stacked in series per phase, the voltage developed across the terminals of any phase will be

$$E_{cj} = S_{j1}V_{dc1}^{j} + S_{j2}V_{dc2}^{j} + \ldots + S_{jn_c}V_{dcn_c}^{j} \qquad (31)$$

where, j=a, b or c represent the phase of the converter. E_{cj} is the product of two vectors, DC voltages across the capacitors and the switching function for that cell. $V_{dcn}{}^{j}$ and S_{jn} represent voltage across the DC capacitor and the switching function for n^{th} cell respectively, where n = 1,2,3,…n_c. Equation (31) can be represented as

$$E_{cj} = \left(S_{j1} + S_{j2} + \ldots + S_{jn_v}\right)\left(\frac{V_{dc1}^{j} + V_{dc2}^{j} + \ldots + V_{dcn_c}^{j}}{n_c}\right) + \Delta E_{cj}$$

$$= S_j V_{dc}^{j} \qquad (32)$$

S_j represents the combined switching function for phase j of the converter. ΔE_{cj} is neglected on assumption that $V_{dcn}^{j} \cong V_{dc}^{j}$.
The fundamental component of switching functions for each of the phases will be

$$S_a = \sqrt{\tfrac{2}{3}}k\sin\left(\omega t + \theta - \delta\right) \qquad (33)$$

$$S_b = \sqrt{\tfrac{2}{3}}k\sin\left(\omega t + \theta - \delta - \tfrac{2\pi}{3}\right) \qquad (34)$$

$$S_c = \sqrt{\tfrac{2}{3}}k\sin\left(\omega t + \theta - \delta - \tfrac{4\pi}{3}\right) \qquad (35)$$

where, $k = \sqrt{\tfrac{3}{2}}\left[\tfrac{4}{\pi}\left(\cos(\alpha_1) + \cos(\alpha_1) + \ldots + \cos(\alpha_{n_c})\right)\right]$.
When the three phase output voltage of the converter are transformed to d-q frame of reference, we arrive at

$$e_{cd} = kV_{dc}\sin\left(\theta - \delta\right) \qquad (36)$$

$$e_{cq} = kV_{dc}\cos\left(\theta - \delta\right) \qquad (37)$$

The variation of voltage across the capacitor of each cell of phase is given by

$$\frac{dV_{dcn}^{j}}{dt} = S_{jn}\frac{i_{cj}}{C_n} \tag{38}$$

Considering a phase of the converter, we can write (38) as

$$\sum_{n=1}^{n_c}\frac{dV_{dcn}^{j}}{dt} = \left(\frac{S_{j1}}{C_1} + \frac{S_{j2}}{C_2} + \ldots + \frac{S_{jn_c}}{C_{n_c}}\right) i_{cj} \tag{39}$$

Equation (39) can be represented as,

$$n_c\frac{dV_{dc}^{j}}{dt} = \left(\frac{S_{j1} + S_{j2} + \ldots + S_{jn_c}}{\sqrt{n_c}}\right)\left(\frac{\frac{1}{C_1} + \frac{1}{C_2} + \ldots + \frac{1}{C_{n_c}}}{\sqrt{n_c}}\right) i_{cj} + \Delta i_{cj}$$

Assuming that the contribution of Δi_{cj} to DC voltage variation is negligible, we arrive at

$$\frac{dV_{dc}^{j}}{dt} = \frac{S_j i_{cj}}{n_c^2 C_{eq}} \tag{40}$$

where, $\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} + \ldots + \frac{1}{C_{n_c}}$. Summing up the variation in DC voltage in all the three phases, using (40), we can write

$$\frac{d}{dt}\left(V_{dc}^{a} + V_{dc}^{b} + V_{dc}^{c}\right) = \frac{S_a i_{ca} + S_b i_{cb} + S_c i_{cc}}{n_c^2 C_{eq}}$$

$$3\frac{d}{dt}V_{dc} = \frac{S_a i_{ca} + S_b i_{cb} + S_c i_{cc}}{n_c^2 C_{eq}} \tag{41}$$

where, $V_{dc} = \sum_{j=a}^{c}\frac{V_{dc}^{j}}{3}$. Rearranging (41), we arrive at,

$$C\frac{dV_{dc}}{dt} = S_a i_{ca} + S_b i_{cb} + S_c i_{cc} \tag{42}$$

where, $C = 3n_c^2 C_{eq}$. Substituting (33) - (35) in (42) we get,

$$C\frac{dV_{dc}}{dt} = k\left(i_{cd}\sin(\theta - \delta) + i_{cq}\cos(\theta - \delta)\right) \tag{43}$$

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X. Biographies

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