Whitepaper

Quick Tips for a Winning Solution for High Bandwidth Network Cards

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Abstract

Ultra-high speed interfaces have become the need of the hour to realize low latency and high throughput networking solutions. These solutions cater to a wide range of high performance applications from stock trading to military radar communication, and require the highest levels of reliability. One of the most practical and common approaches to designing such a solution is using Field Programmable Gate Array (FPGA) with integrated serial transceivers. In this paper, we will explore some simple and quick ways of designing an effective solution, while also addressing the following key challenges:

Constraints on size Achieving XMC/PCIe form factor while packing a FPGA along with other required components such as DDR SDRAM devices, QSFP/SFP connector, clock devices and power circuitry	**Optimality of clock design** Working out the most optimum clock design which meets all the clock requirements of FPGA and other major components in the minimum area and lowest cost
Complexities in power design Meeting each component's multiple voltage and current requirements along with their individual sequencing requirements	**Thermal requirements of FPGA** Meeting the height restrictions of XMC/PCIe form factor limits the heat dissipation mechanism for the FPGA

Form Factor

1. A rough placement diagram of all the major components can be done initially to arrive at the overall size. The position of FPGA should be fixed and banks should be allocated such that fan out of signals to other components is straight forward. Sufficient space should be given between the components considering the signal routing constraints.

2. Form factors like XMC/PCIe have height restrictions including the thickness of the PCB. This in turn demands optimized design of the PCB Stack-up with following considerations:
    a. The stack-up should have enough plane layers and corresponding signal layers considering fan out of the FPGA signals with good Signal Integrity.
    b. PCB material selection is critical from the dielectric loss & highest signal frequency perspective.

    For example, for 28Gbps operation, Megtron 6 PCB dielectric can be used and an example stack-up for 16-Layer is given here in Figure 1.

Figure 1: Stack-up for 16-Layer PCB

3. Routing of all major interfaces should be worked out in advance to avoid delays and rework. All high speed lanes should be routed preferably in outer layers. Pre and Post Layout Signal Integrity analysis of high speed interfaces with right set of tools needs to be considered.

Clock Design

1. Each FPGA has its own clock input design considerations, such as jitter specifications, based on the transceiver interface frequency. It is also recommended to ensure additional optimization. For instance, one clock can drive the adjacent transceiver lanes to reduce the cost and also save the PCB area.

2. Considerations such as bit-stream loading time and boot requirement for interface like PCIe should be taken into account for selecting the right clock input for the FPGA.

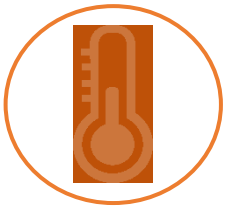
Power Design

1. Preference should be given to power ICs that have low footprint (take less board area) with multiple outputs. Also consideration needs to be given for output ripple, line and load regulation.

2. For meeting core current requirements of FPGA, which may be in order of 30A and more, it is recommended to use devices in parallel configuration as it provides better load and line regulations than using a single device.

3. It is better if power supply ICs have UVLO (Undervoltage-Lockout) option as these can be used for implementing power sequencing.

Thermal Analysis



1. It is recommended to do thermal analysis for the FPGA and work out the corresponding heat spreading mechanism such as passive or active heatsinks. These heatsinks can be mounted on the PCB and thus provision should be made on the board during the layout stage.

2. In form factors such as XMC/PCIe with restricted height, the volume of the heatsink and thereby better thermal dissipation can be achieved by increasing the dimensions of the heatsink in length and breadth.

At Ittiam, we have been successful in addressing these challenges and delivering highly reliable system designs for worldwide OEMs/ODMs. If you are interested in discussing your product requirements, do write to us at ids-mkt@ittiam.com

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About the Author

Ayusman Mohanty brings in around eight years of experience, of which he has spent six years at Ittiam, with key focus on building hardware and RTL for video broadcast and surveillance systems. He currently works as Principal Engineer, Media Server Technologies – Systems (MSTS), leading multiple hardware and RTL projects based on TI Sitara™ and Xilinx's UltraScale™ FPGAs. Ayusman also leverages his system expertise to contribute towards device drivers whenever needed. He has a B.Tech degree from the National Institute of Technology, Kurukshetra.

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