Whitepaper

Signal Integrity Simulation for High Speed PCB Design

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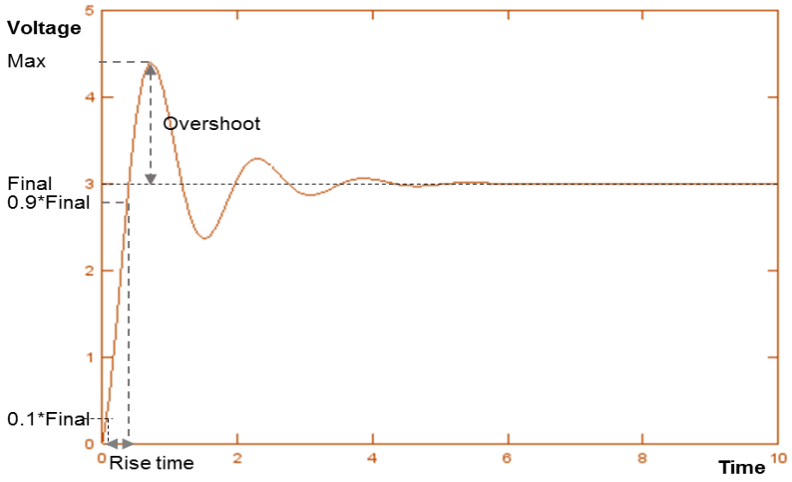
Abstract

This paper provides an overview of the need for signal integrity (SI) simulations in high speed Printed Circuit Board (PCB) design. It details the procedure to perform signal integrity simulations along with the pre-layout and post-layout stages of signal integrity simulations during the PCB design.

What is SI Simulation?

Signal Integrity (SI) refers to the quality of a signal. It is the measure of the shape of a signal using key parameters such as rise time, fall time, high level voltage, low level voltage, overshoot and undershoot.



Signal integrity issues refer to any deviation in these parameters from the values specified in the datasheet of the corresponding device. The issues may occur due to various reasons such as transmission line effects, cross-talk or attenuation. Signal integrity simulation refers to observing these behaviors using relevant software tools.

Need for SI Simulation

The signal integrity of **high speed interfaces such as DDR4, PCIe Gen4** or **QSFP28** is one of the most critical parameters for it to work as intended**.** With the current trend towards higher frequency, higher rise and fall times and more dense circuits, signal integrity has become more critical than ever.

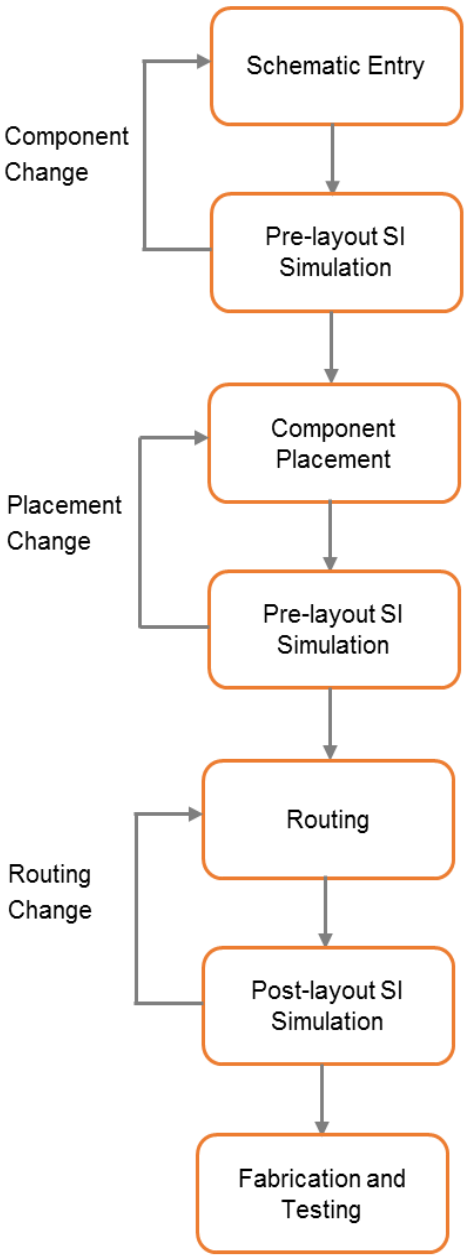
Any form of signal integrity issue in the testing stage can lead to re-design of the hardware. Since the cost of re-design and the time lost in the process is substantial, it is always recommended to proactively perform signal integrity simulations. **Signal integrity simulation tools not only check for issues, but also suggest relevant changes to resolve the issues.**

When Do We Perform SI Simulation?

SI simulation is performed mainly at two stages of the PCB design: **Pre-layout** and **Post-layout**.

Pre-layout SI simulation is carried out on completion of the schematic entry, before proceeding to the layout stage. Pre-layout simulations suggest overall design feasibility and constraints. These include stack-up, dielectric material (like FR4, Megtron, EM-888), preferred routing layer, maximum number of vias, via structure, type of via (through hole or with back-drill), trace impedance and maximum trace length to be followed during the layout stage.

This simulation also provides recommendations for an appropriate termination to be used (like series termination, parallel termination, AC/DC coupling) along with the values. The Pre-layout SI may be performed before or after the component placement completion depending on the criticality of the interface and the time involved in re-doing the component placement.



Post-layout SI simulation is performed after the layout is complete based on recommendations from the pre-layout SI simulation. Post-layout SI simulation is typically performed as a final review of signal integrity of the various interfaces. It helps ensure that the specifications in the respective device datasheets or those provided by various standard bodies are met. In this case, the layout is closed and all the actual data such as trace lengths, trace width, trace spacing, layers used for routing, stack-up and number of vias are available.

Therefore, the results from the post-layout SI simulations are closer to the actual values and give a fair idea of how much margin is available from the specifications. The margin is required, as there can be small differences in simulated and actual values. If there are any deviations from the specifications, a minor layout change may be required to resolve the same. In such cases, the post-layout SI simulation must be repeated after the updates to confirm if the deviations have been addressed.

The SI Simulation Process

There are several software packages available to perform SI simulation. These include the following:

- ANSYS SIwave
- Keysight ADS
- Mentor Hyperlynx

These tools require one or more of the following files as input to perform SI simulations:

- Circuit schematics with complete net list
- Bill of materials capturing the manufacturer and manufacturer part number of all parts
- Stack-up including trace width/separation and dielectric details
- PCB layout with routing and power/ground planes
- IBIS/IBIS-AMI models and/or S-parameter models of various components/connectors used, and the appropriate sub-model selected
- Signals/interfaces to be analyzed and the corresponding frequency of operation
- Datasheet and/or standard documents to be referred for required specifications

Here are the output files from the SI simulations:

- **Eye-diagram analysis:** The eye-diagram is obtained by the super-position of all possible signal switching sequences over a large period of time. Higher eye-opening area indicates better quality of the signal. The critical parameters provided by the eye-diagram is eye-height and eye-width and these are compared against the interface specifications.
- **Cross-talk analysis:** Cross-talk refers to distortion in a signal waveform due to undesired capacitive coupling from an adjacent high frequency signal. While cross-talk between any two adjacent signals running at high frequency is common, interface specifications allow a certain amount of cross-talk noise. Cross-talk analysis indicates whether the trace to trace clearance on PCB needs to be increased in order to meet this specification.
- **S-parameter loss analysis:** It provides the insertion loss and return loss values over a frequency range measured at the destination.
- **Maximum length analysis:** It provides the maximum trace length allowed on the PCB for a signal, based on the voltage drop at destination and the drive strength at source.

- **(Via) Impedance analysis:** This reflects the maximum number of vias and their appropriate size required to minimize the transmission line effects caused by impedance discontinuity in the signal path.

The software packages take the required input files and generate the various output files. These output files are analyzed by the user and compared with the specifications. If there are any deviations, the user needs to perform a few layout changes based on prior knowledge or in line with the recommendations provided by the simulation tools, if any. Thereafter, the simulation needs to be re-run and the SI verified again.

Conclusion

Signal integrity simulation is an integral part of any high speed PCB design. It helps in anticipating and eliminating critical design issues in the early stages of PCB design, thereby saving time and cost involved in debugging issues and re-designing the PCB. The best practice is to perform SI simulation at the pre-layout stage for any new design involving high speed interfaces. However, if the design is based on already validated PCBs, we can skip the pre-layout step and directly perform a post-layout simulation.

About the Author

Raja Ashutosh Kedia is a Senior Engineer in the Media Server Technologies – Systems business unit at Ittiam. He has been a part of the company for around five years, focusing primarily on hardware and RTL design projects based on TI's Sitara family of processors, Socionext SoCs, Xilinx's UltraScale and Intel's Cyclone family of FPGAs. He has a B.Tech degree in Electrical Engineering from the Indian Institute of Technology, Roorkee.

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